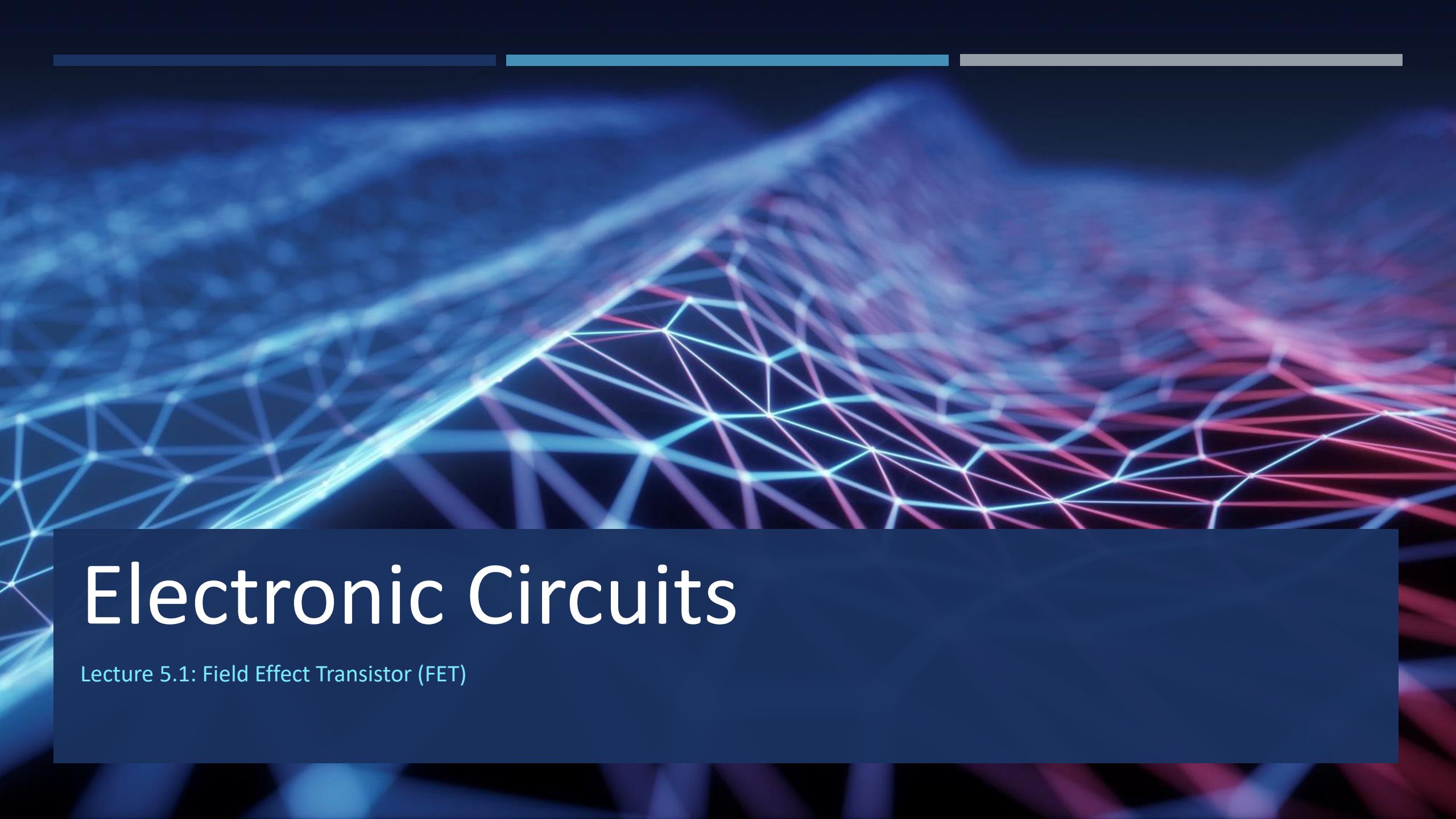
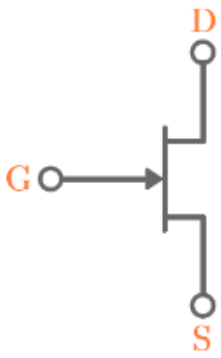
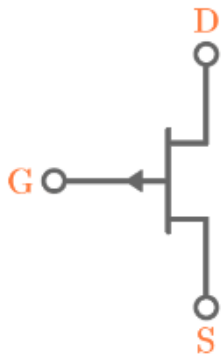
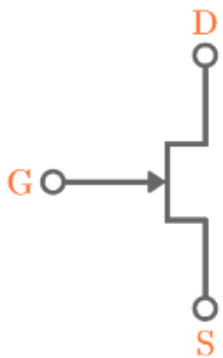


Electronic Circuits

Lecture 5.1: Field Effect Transistor (FET)

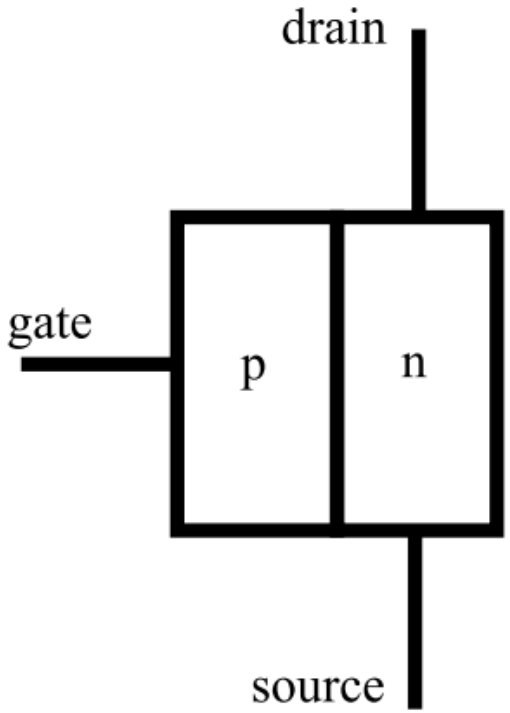
Field Effect Transistors (FETs)

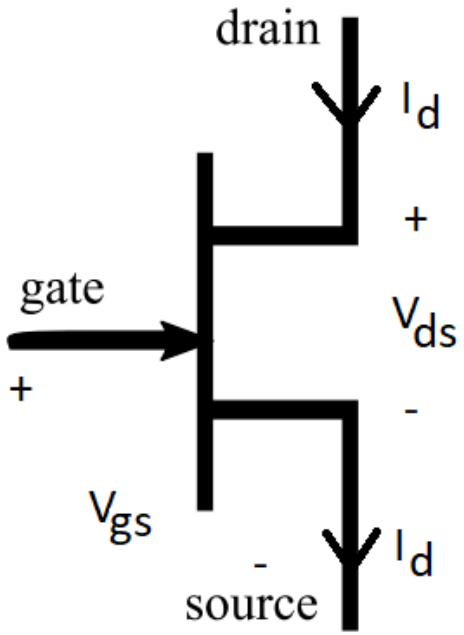
JFET	MOSFET		MESFET
	(Depletion)	(Enhancement)	(n-channel)
			
n-channel	n-channel	n-channel	Depletion
			
p-channel	p-channel	p-channel	Enhancement

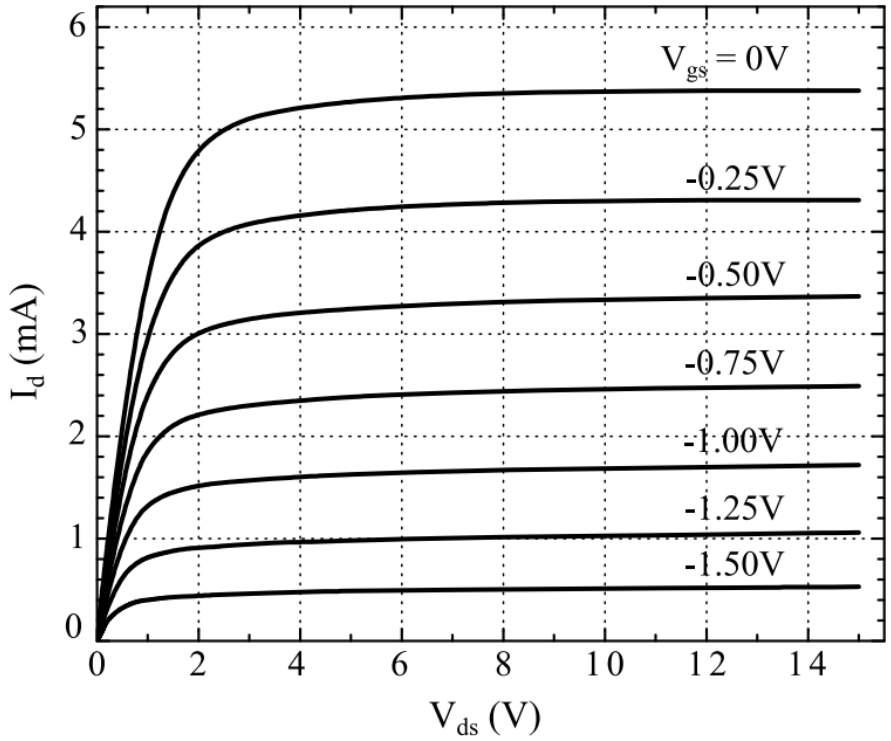
Formulas

Drain Current	$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
Gate to Source Voltage	$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$
Power Dissipation	$$P_D = V_{DS}I_D$$
Resistance at a particular level of V_{GS}	$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$
Drain Current (MOSFET/MESFET Enhancement type)	$$I_D = k\left(V_{GS} - V_T\right)^2$$ $$k = \frac{I_{D(ON)}}{\left(V_{GS(ON)} - V_T\right)^2}$$

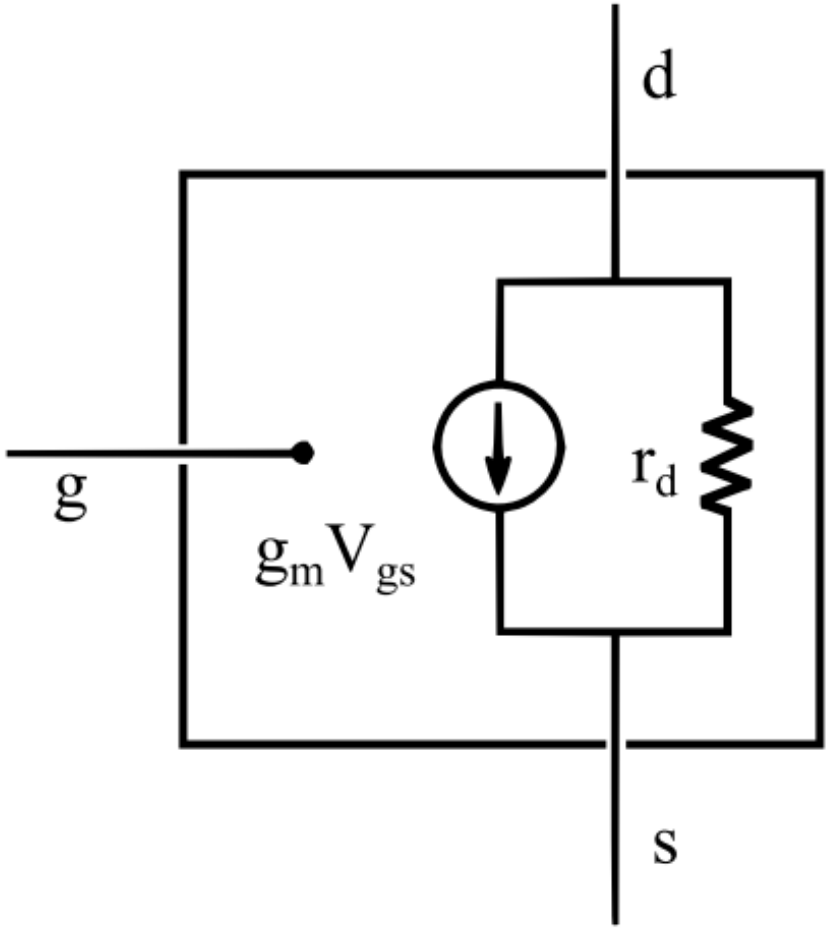
N-Channel FET







N-Channel FET (AC Equivalent Circuit)



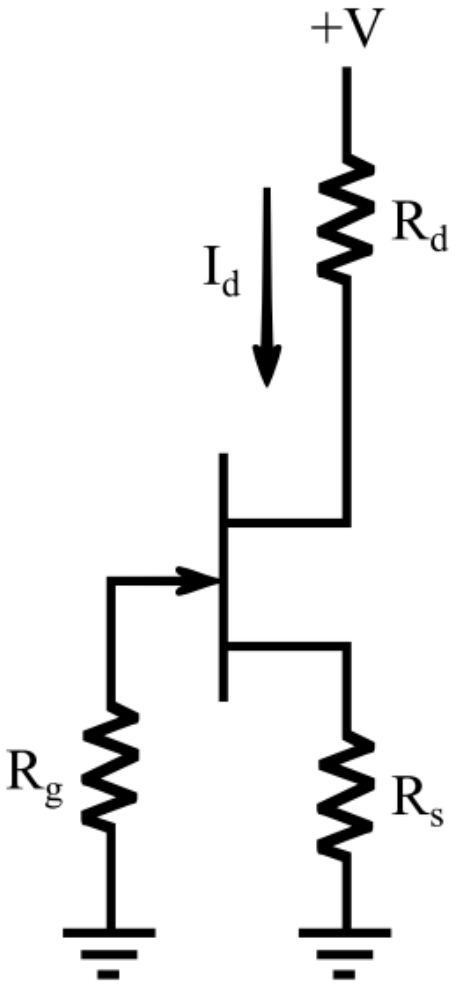
gate – source ~ open circuit

$$I_d = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2$$

$$g_m = \left.\frac{dI_d}{dV_{gs}}\right|_{V_{ds}\ at\ operating\ point}$$

$$r_d = \left.\frac{dV_{ds}}{dI_d}\right|_{V_{gs}\ at\ operating\ point}$$

FET Analysis Example #1: DC Analysis



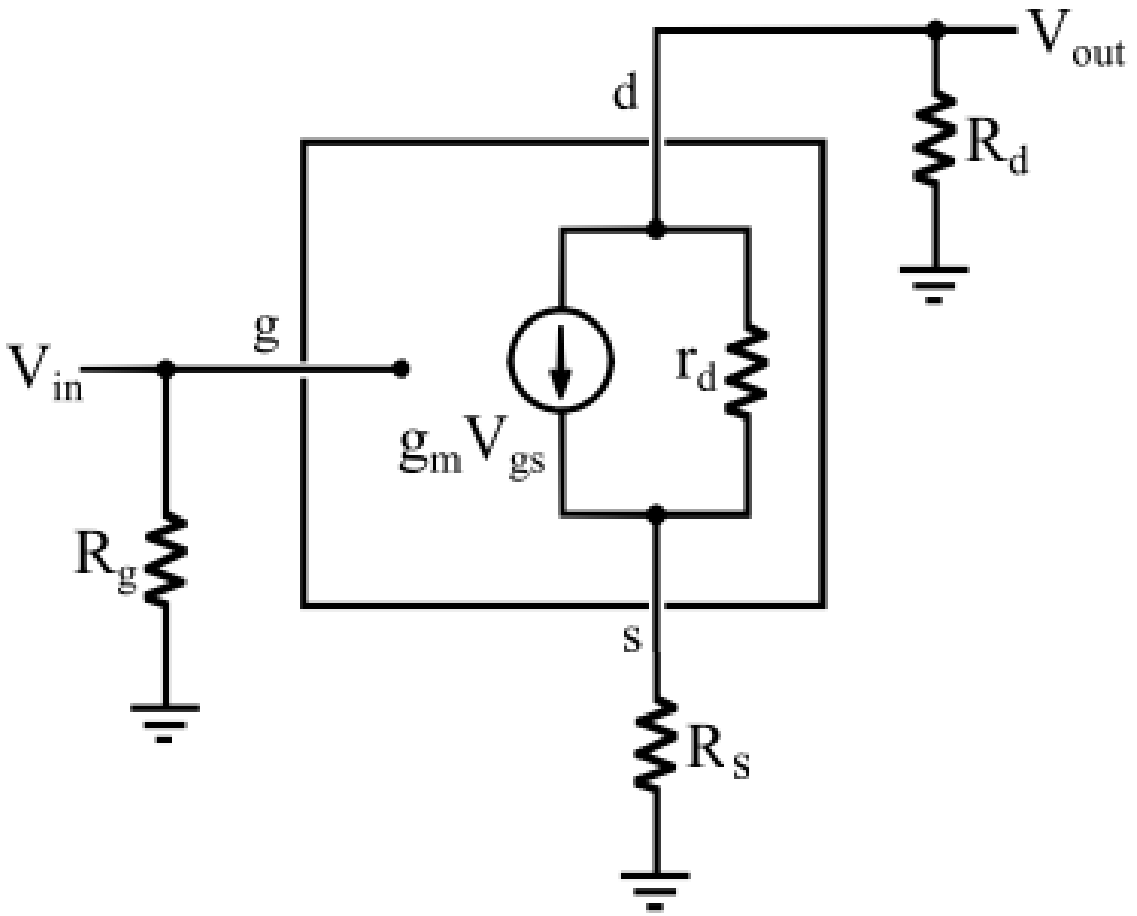
$$R_g * 0 + V_{gs} + R_s * I_d = 0$$

$$I_d = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2$$

$$I_d - I_{dss}\left(1 + \frac{R_s * I_d}{V_p}\right)^2 = 0$$

We can find I_d, V_{gs}, V_{ds}, and in general, V_d is the output point.

FET Analysis Example #1: AC Analysis



$$V_{out} = -R_d * I_d$$

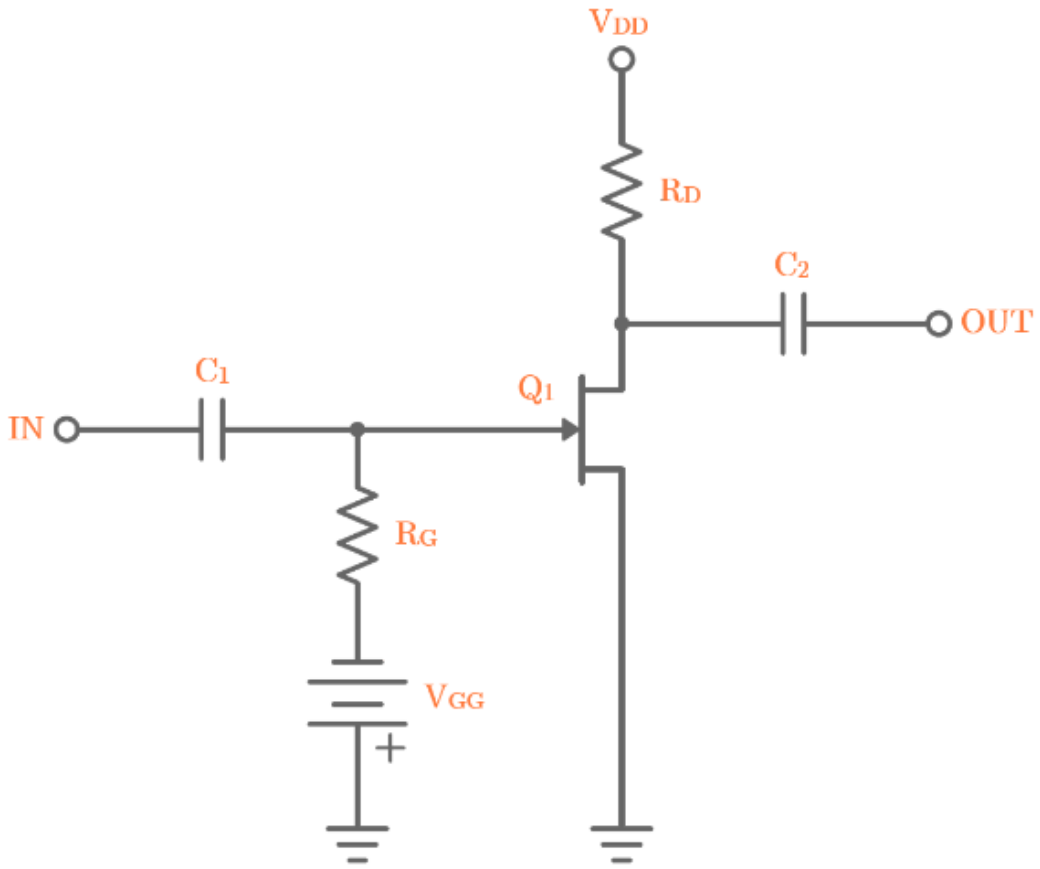
$$V_{out} = r_d * (I_d - g_m * V_{gs}) + R_s * I_d$$

$$V_{in} = V_{gs} + R_s * I_d$$

$$V_{in} = V_{gs} - R_s * \frac{V_{out}}{R_d}$$

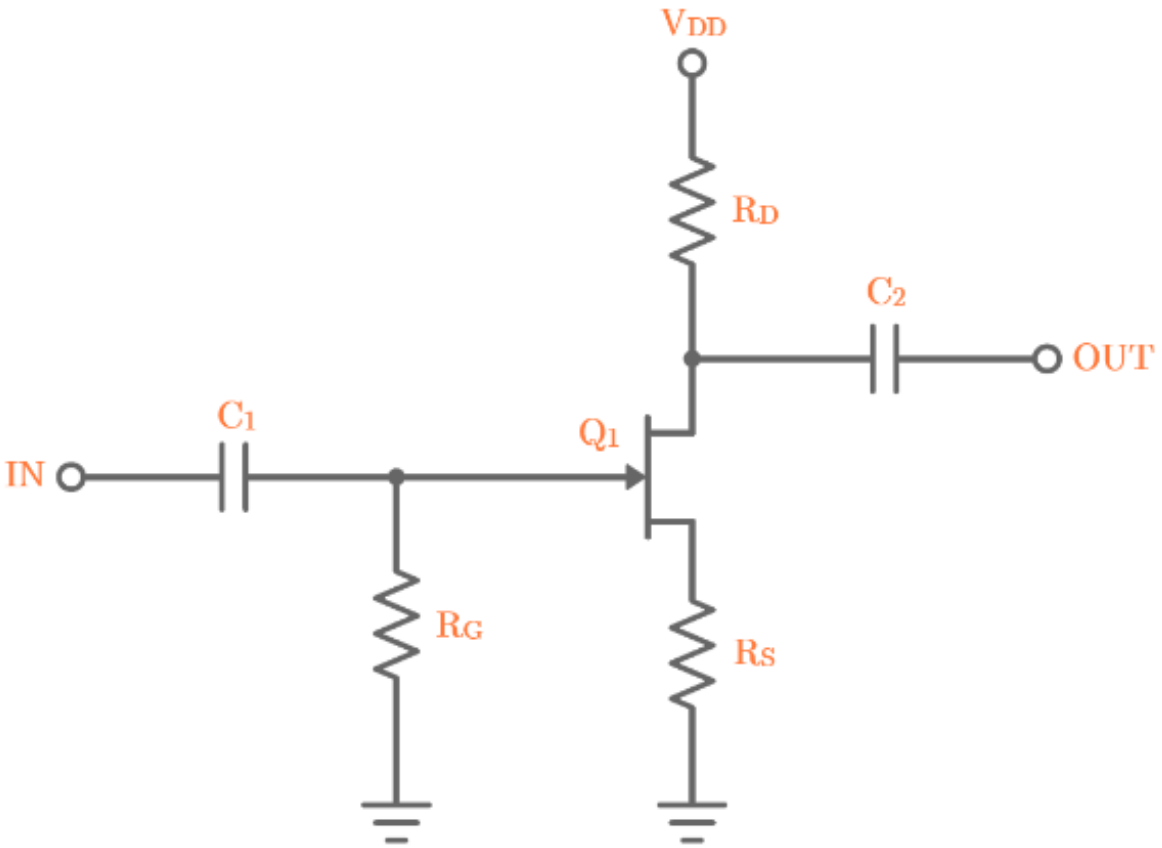
We can find V_{gs}, V_{ds}, I_d, and in general, V_d is the output point.

Fixed-Bias Configuration



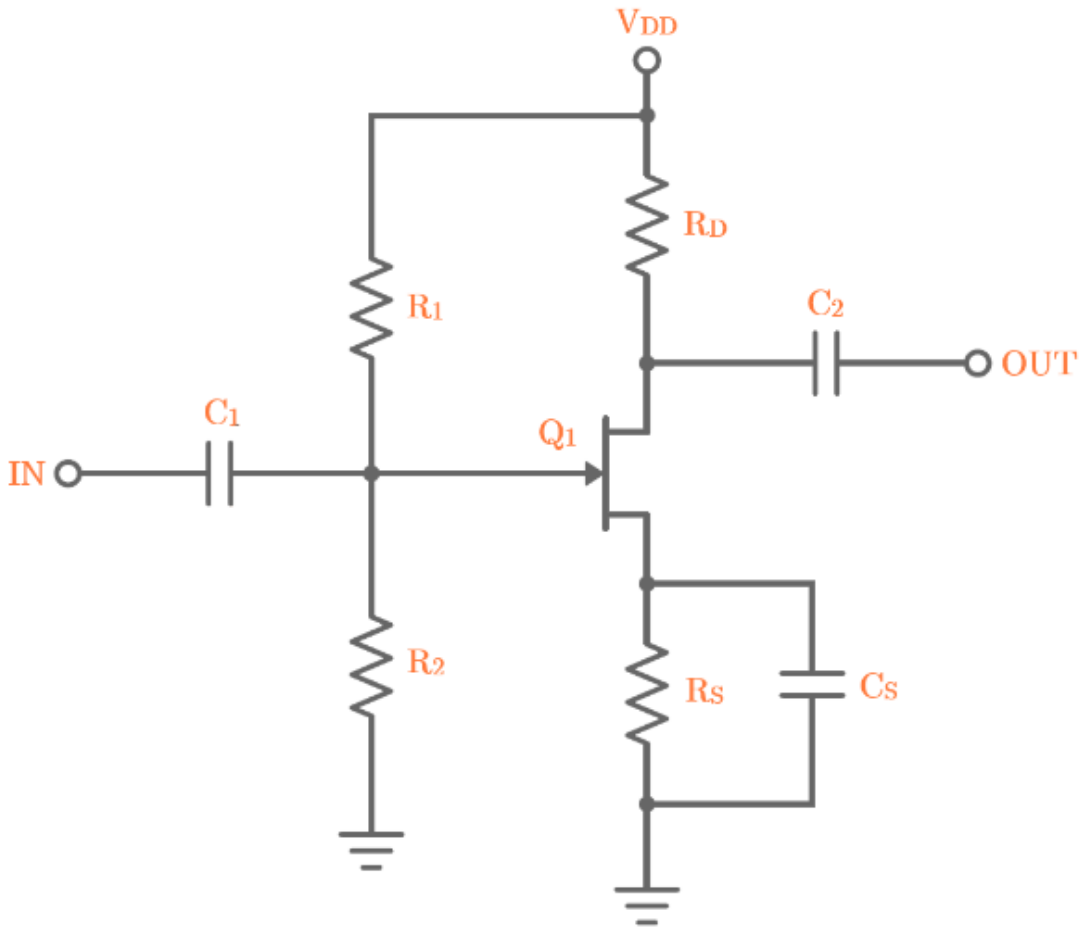
Gate to Source Voltage	$V_{GS} = -V_{GG}$
Drain to Source Voltage	$V_{DS} = V_{DD} - I_D R_D$

Self Bias Configuration



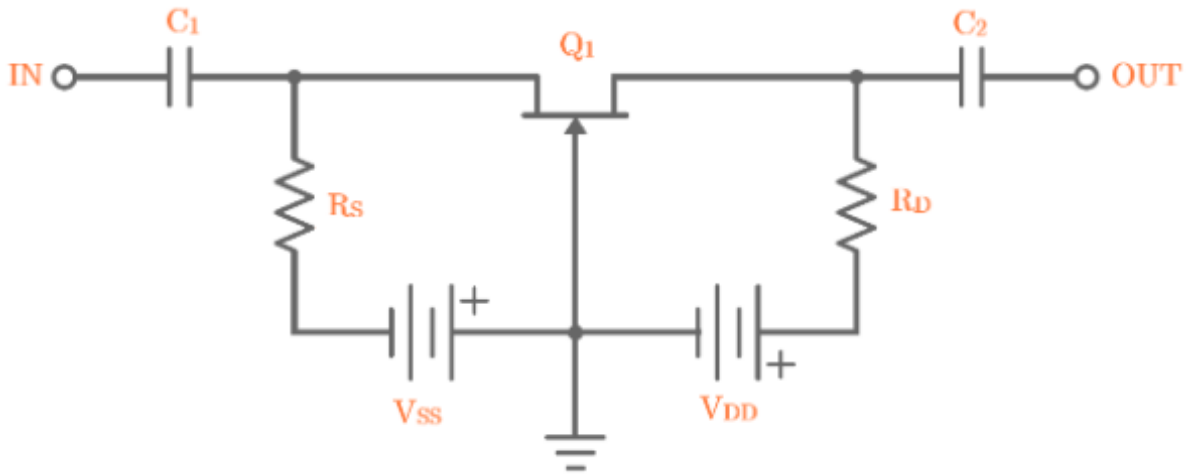
Gate to Source Voltage	$V_{GS} = -I_D R_S$
Drain to Source Voltage	$V_{DS} = V_{DD} - I_D (R_S + R_D)$

Voltage-Divider Bias Configuration



Gate Terminal Voltage	$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$
Gate to Source Voltage	$V_{GS} = V_G - I_D R_S$
Drain to Source Voltage	$V_{DS} = V_{DD} - I_D (R_S + R_D)$

Common Gate Configuration



Gate to Source Voltage	$V_{GS} = V_{SS} - I_D R_S$
Drain to Source Voltage	$V_{DS} = V_{DD} + V_{SS} - I_D (R_S + R_D)$

Thanks for listening ☺

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