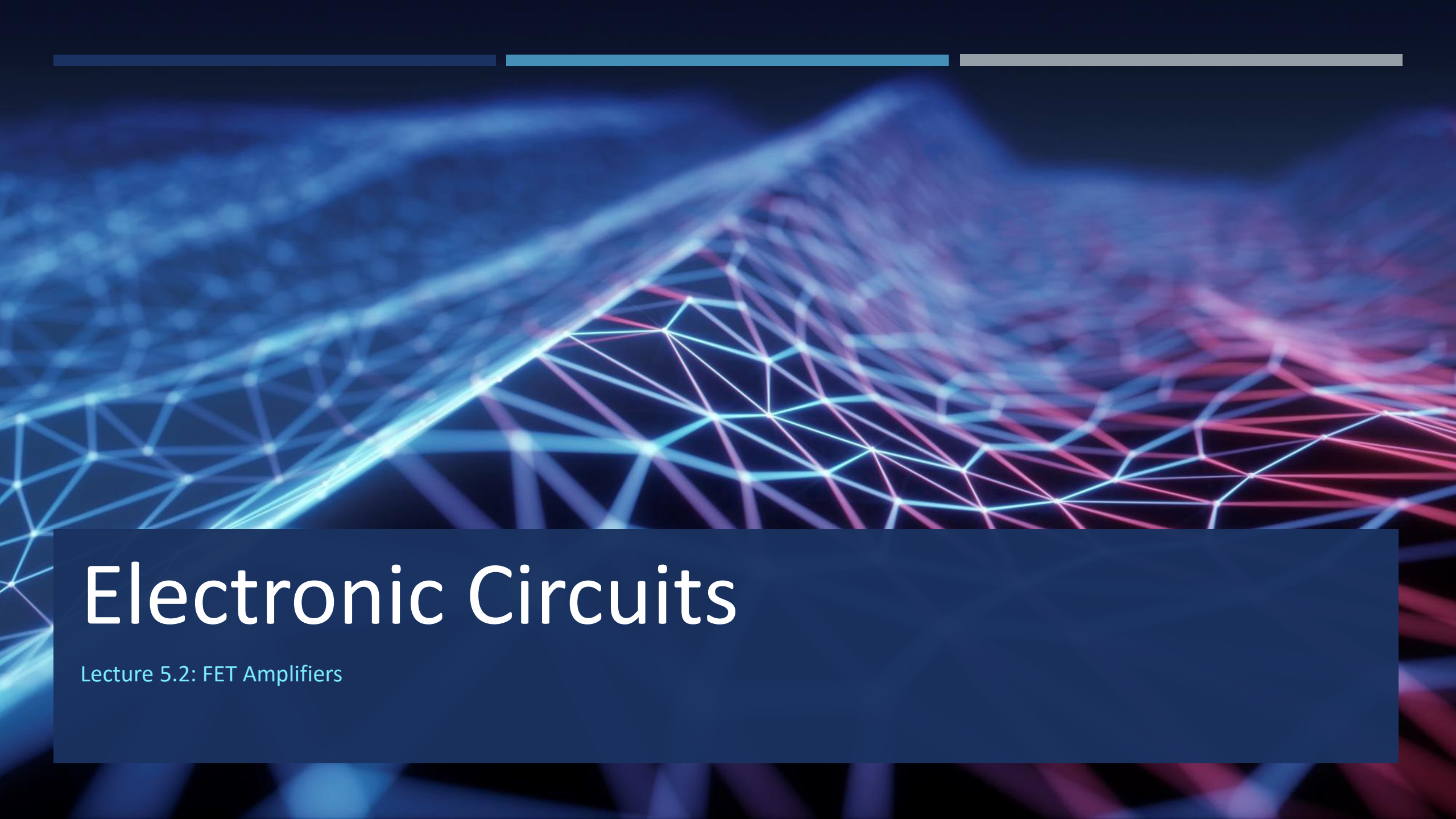
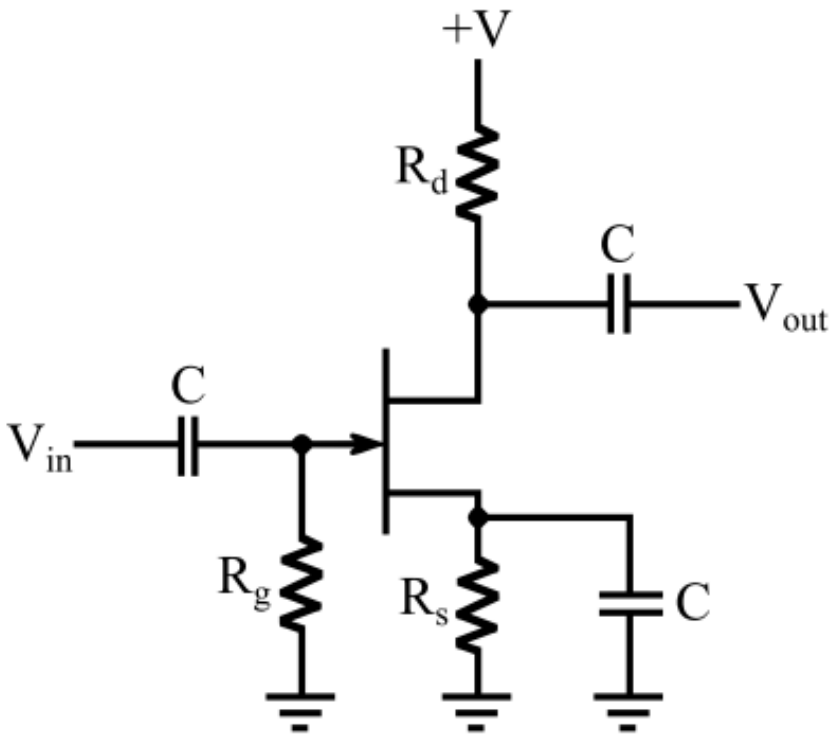


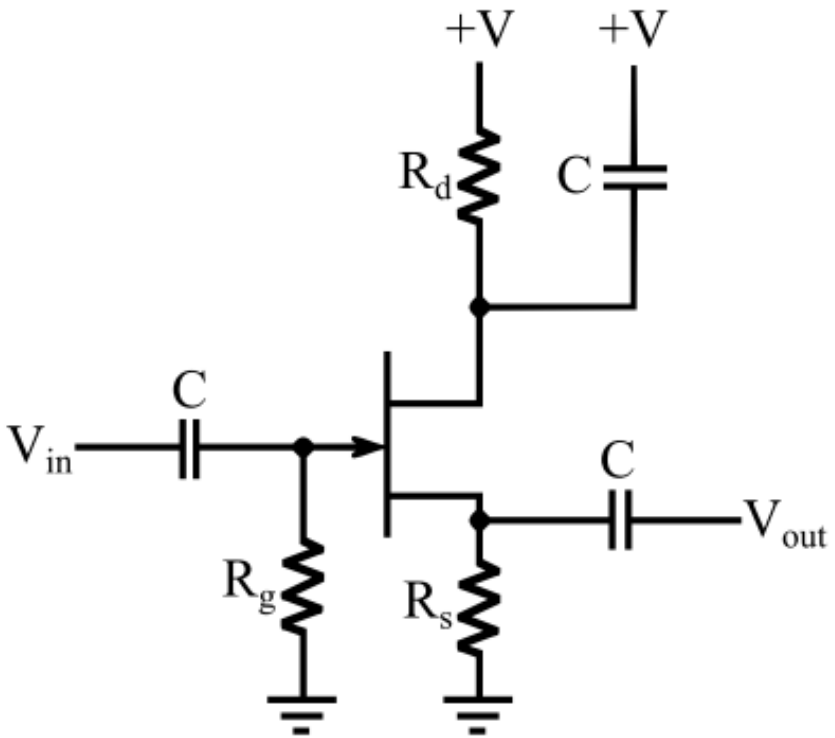
Electronic Circuits

Lecture 5.2: FET Amplifiers

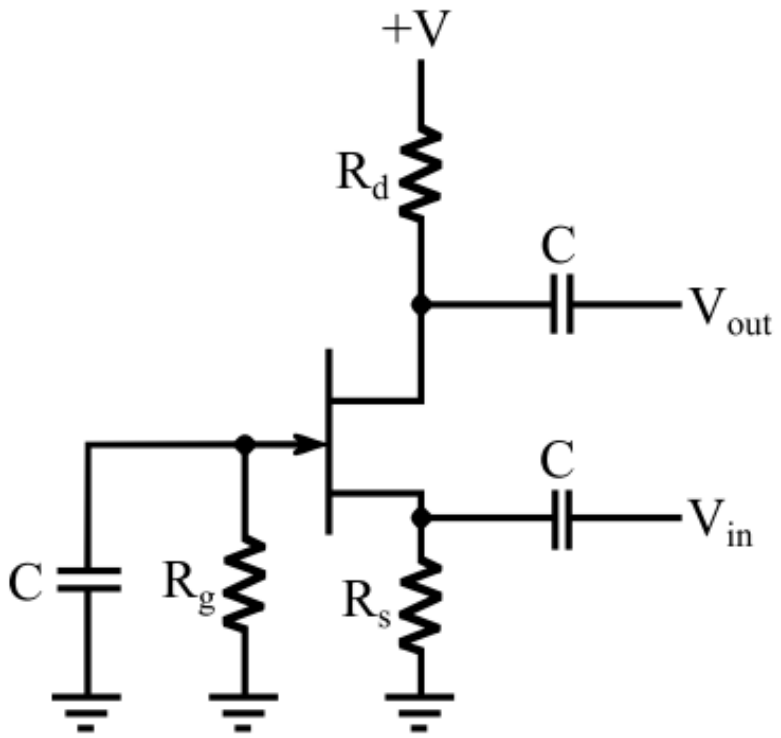
Basic FET Amplifiers



Common Source

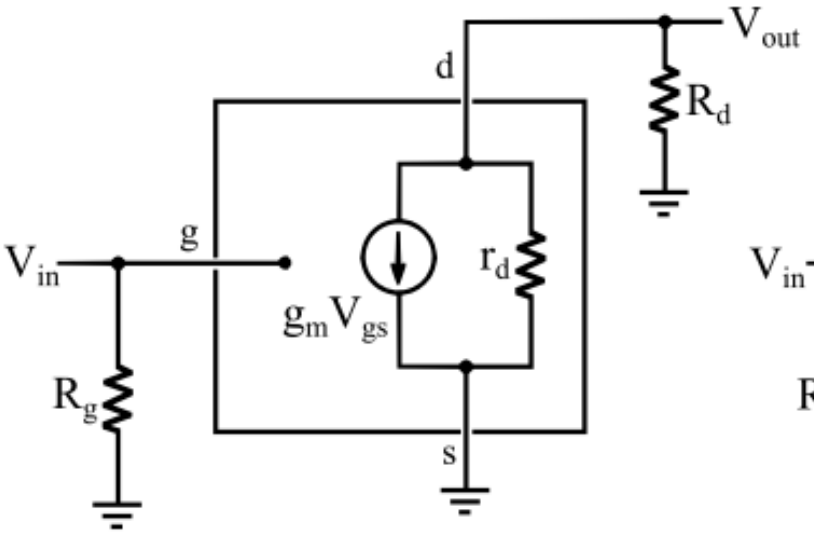


Common Drain
(Source Follower)

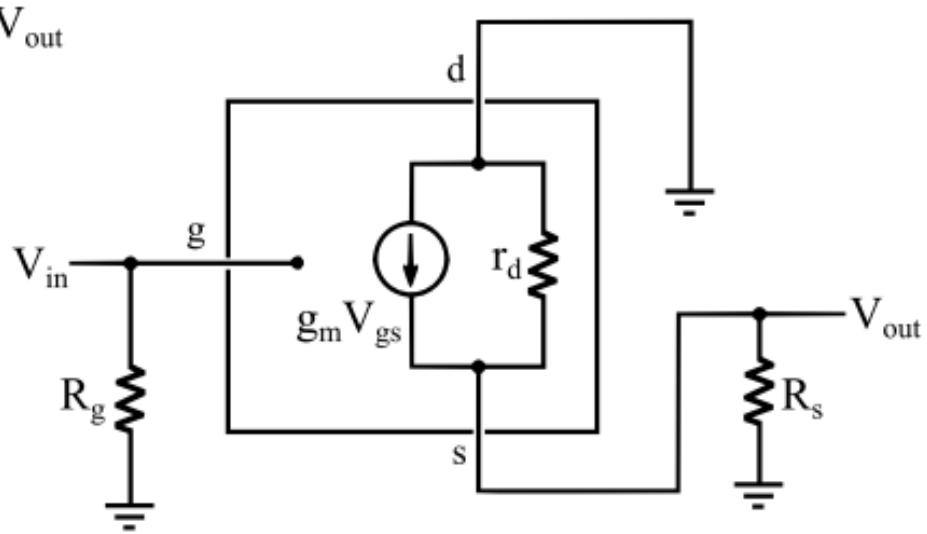


Common Gate

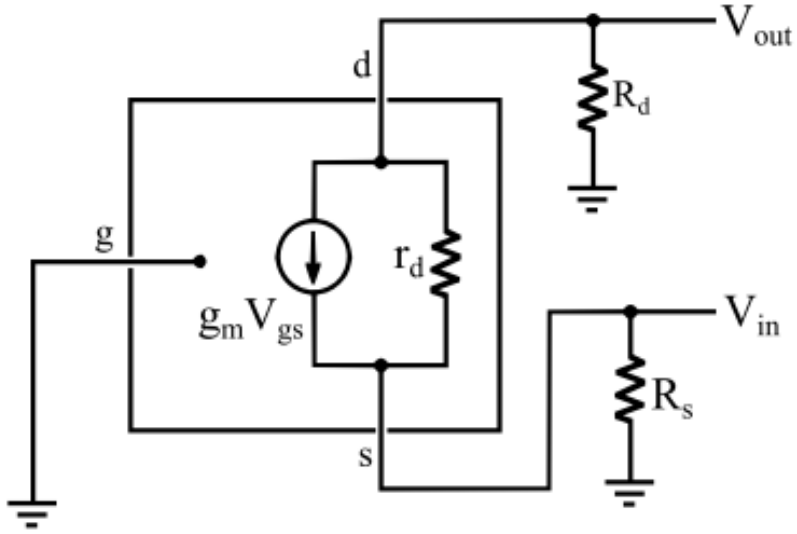
Basic FET Amplifiers (AC Equivalents)



Common Source



Common Drain

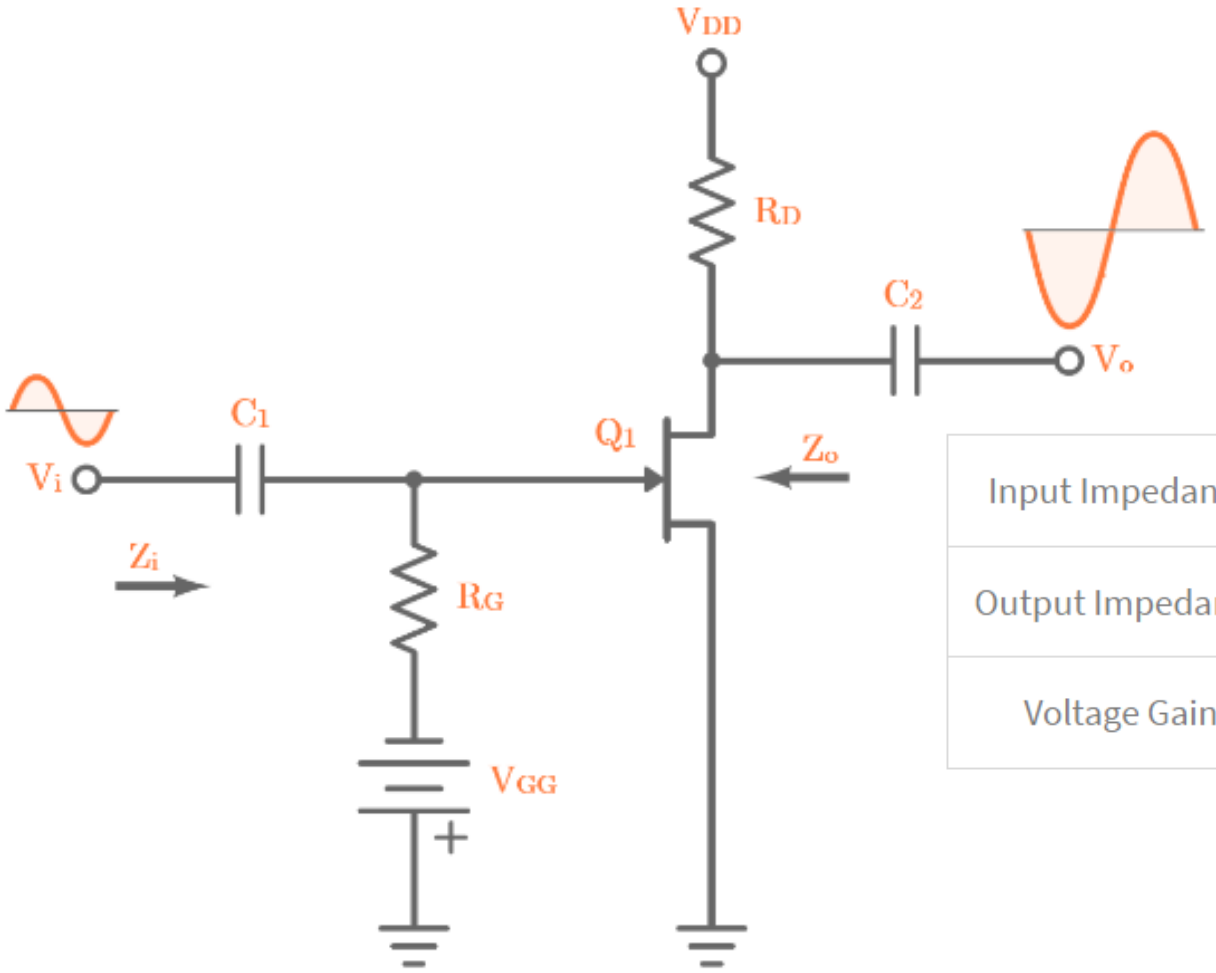


Common Gate

FET Transconductance Factor

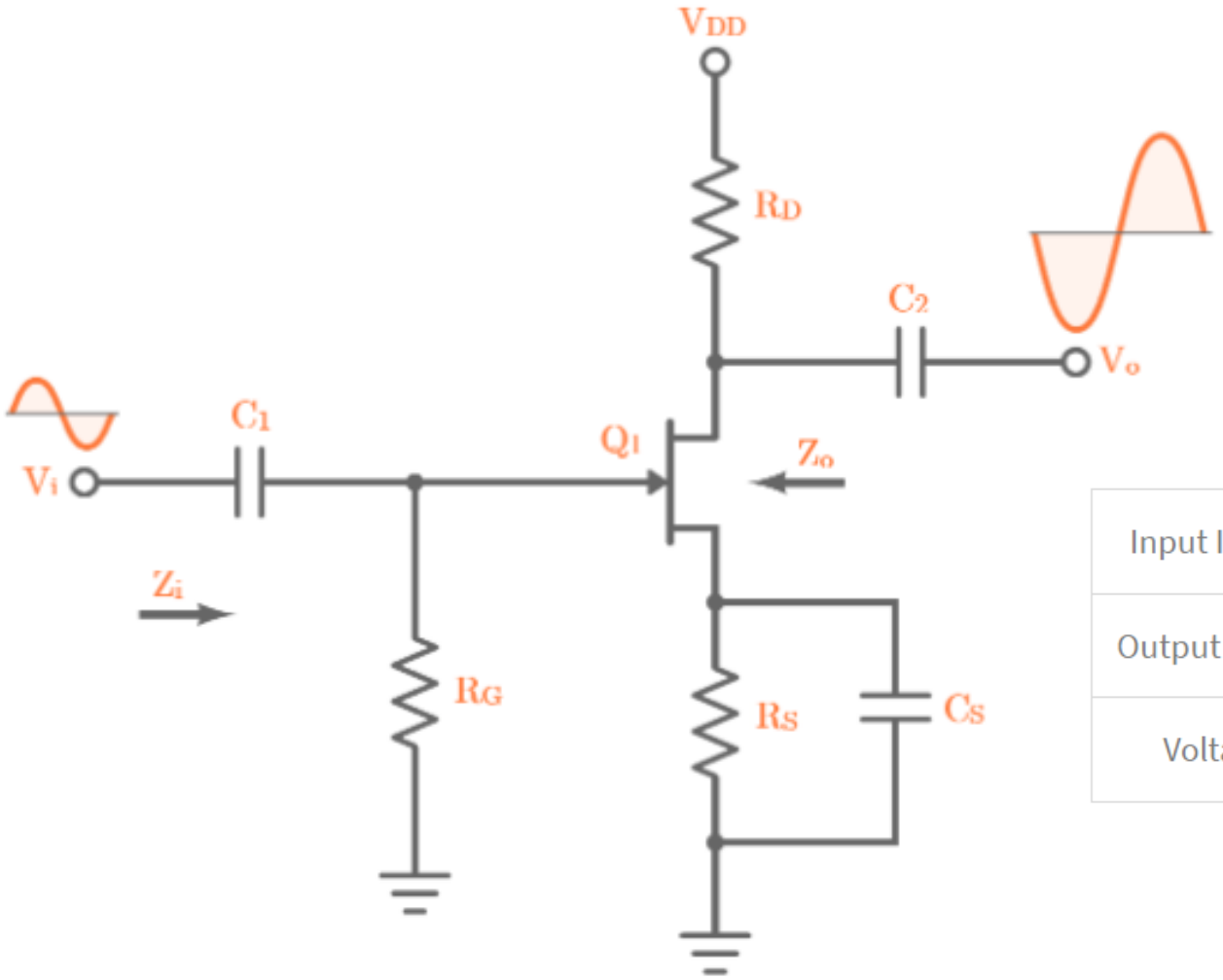
$$g_m = y_{fs} = \frac{\Delta \mathrm{I_D}}{\Delta \mathrm{V_{GS}}} = g_{m_0}\left[1 - \frac{\mathrm{V_{GS}}}{\mathrm{V_P}}\right] = g_{m_0}\sqrt{\frac{\mathrm{I_D}}{\mathrm{I_{DSS}}}}\,, \qquad g_{m_0} = \frac{2\mathrm{I_{DSS}}}{|\mathrm{V_P}|}$$

JFET or D-MOSFET Fixed-Bias Configuration (No-Load)



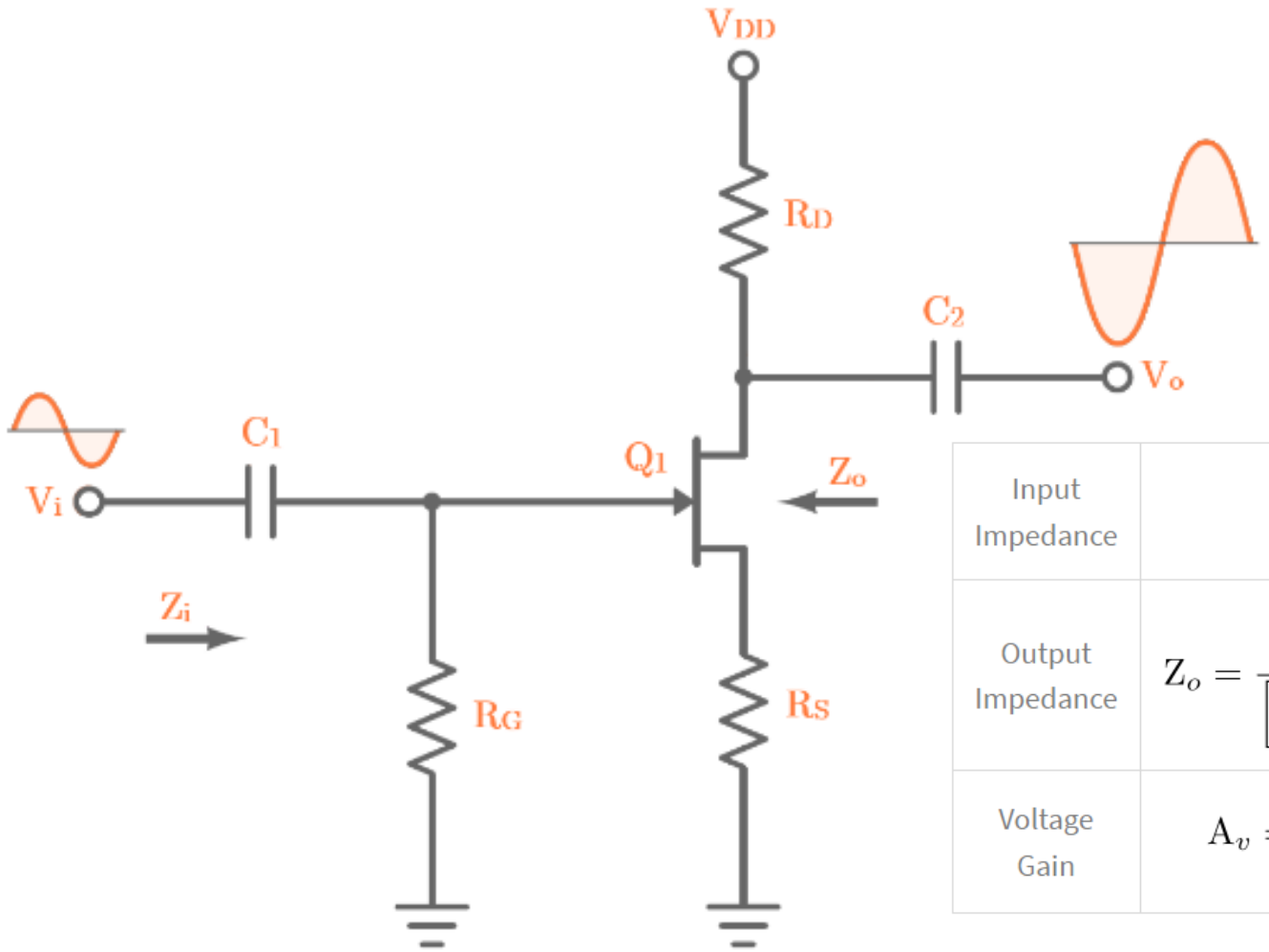
Input Impedance	$\mathrm{Z}_i = \mathrm{R_G}$	
Output Impedance	$\mathrm{Z}_o = \mathrm{R_D} \parallel \mathrm{r}_d$	$\mathrm{Z}_o \cong \mathrm{R_D} \quad (\mathrm{r}_d \geq 10\mathrm{R_D})$
Voltage Gain	$\mathrm{A}_v = -g_m\,(\mathrm{r}_d \parallel \mathrm{R_D})$	$\mathrm{A}_v \cong -g_m\mathrm{R_D} \quad (\mathrm{r}_d \geq 10\mathrm{R_D})$

JFET or D-MOSFET Self-Bias Configuration Bypassed RS (No-Load)



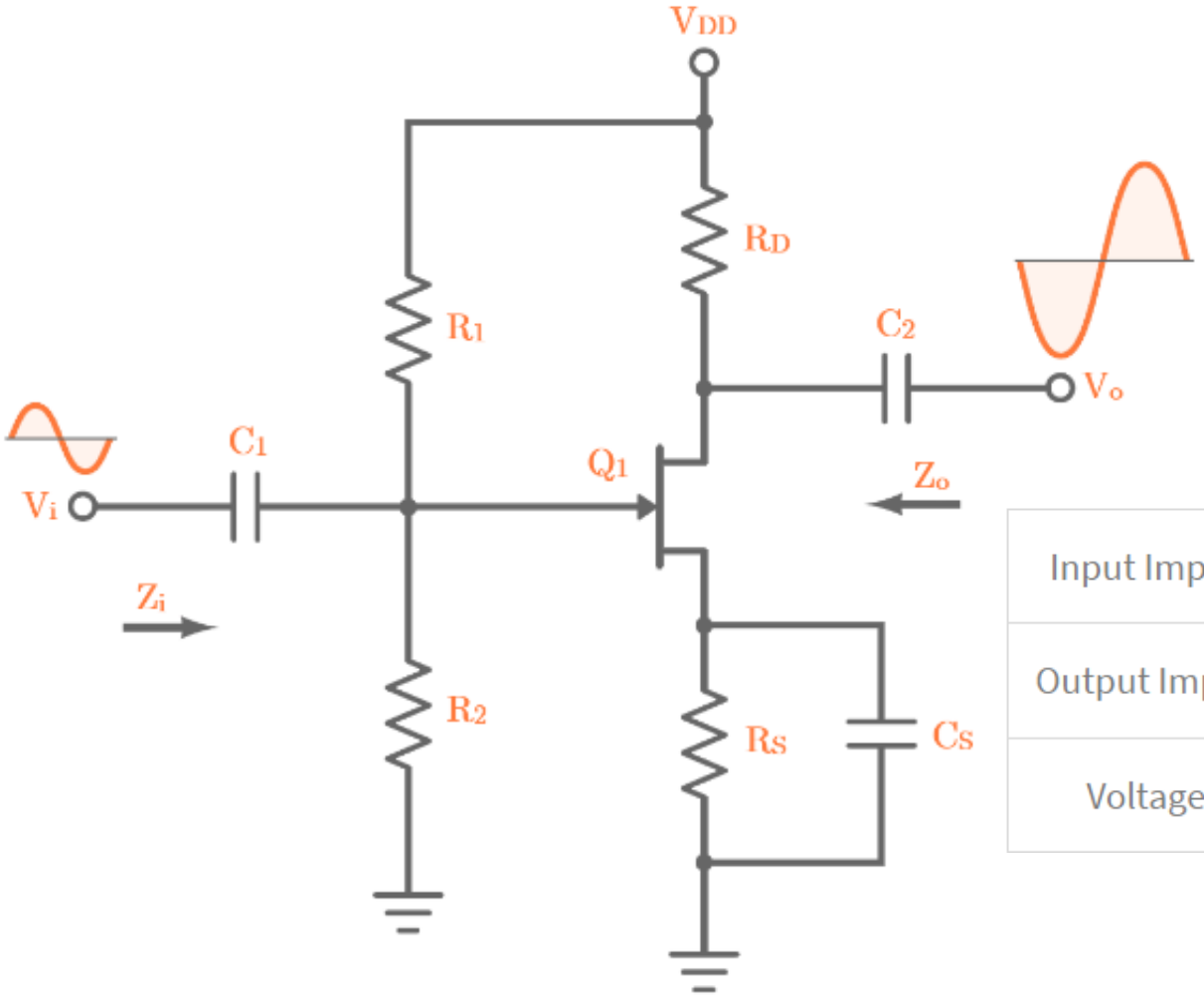
Input Impedance	$\mathrm{Z}_i = \mathrm{R}_\mathrm{G}$	
Output Impedance	$\mathrm{Z}_o = \mathrm{R}_\mathrm{D} \parallel \mathrm{r}_d$	$\mathrm{Z}_o \cong \mathrm{R}_\mathrm{D} \quad (\mathrm{r}_d \geq 10\mathrm{R}_\mathrm{D})$
Voltage Gain	$\mathrm{A}_v = -g_m \left(\mathrm{r}_d \parallel \mathrm{R}_\mathrm{D}\right)$	$\mathrm{A}_v \cong -g_m \mathrm{R}_\mathrm{D} \quad (\mathrm{r}_d \geq 10\mathrm{R}_\mathrm{D})$

FET or D-MOSFET Self-Bias Configuration Unbypassed RS (No-Load)



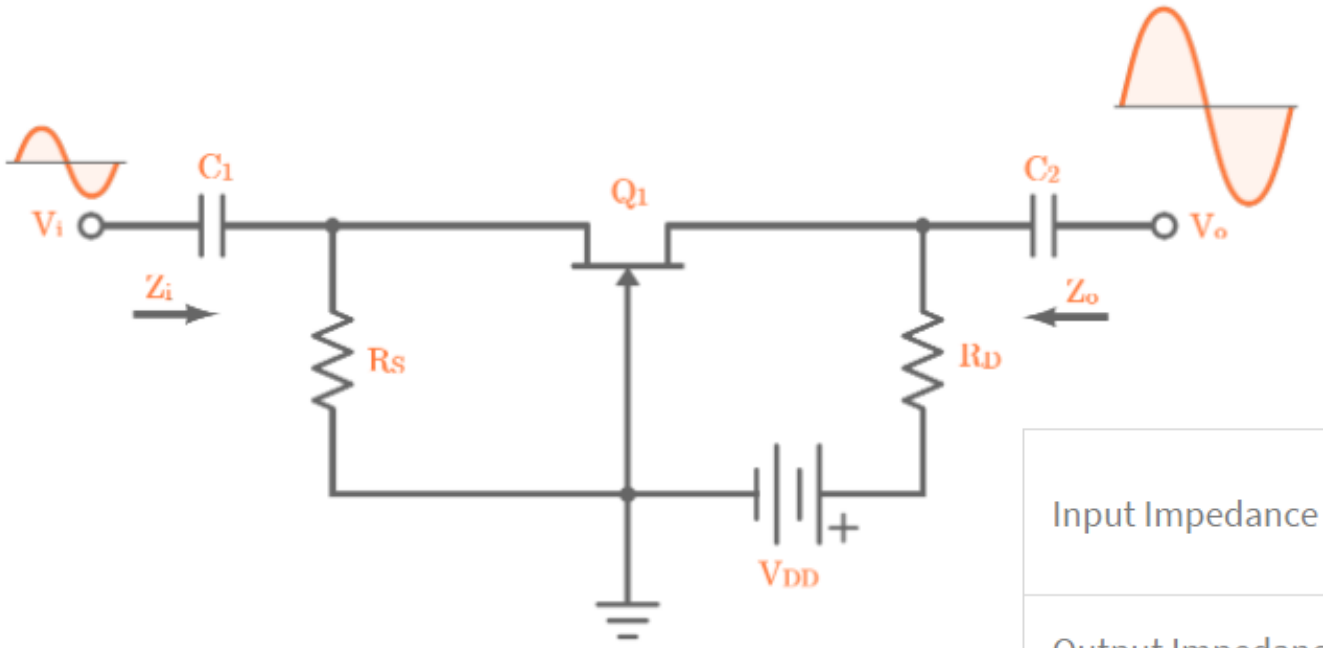
Input Impedance	$Z_i = R_G$	
Output Impedance	$Z_o = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]} R_D$	$Z_o = R_D \quad (r_d \geq 10R_D \; or \; r_d = \infty\,\Omega)$
Voltage Gain	$A_v = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$	$A_v = -\frac{g_m R_D}{1 + g_m R_S} \quad [r_d \geq 10(R_D + R_S)]$

JFET or D-MOSFET Voltage-Divider Bias Configuration (No-Load)



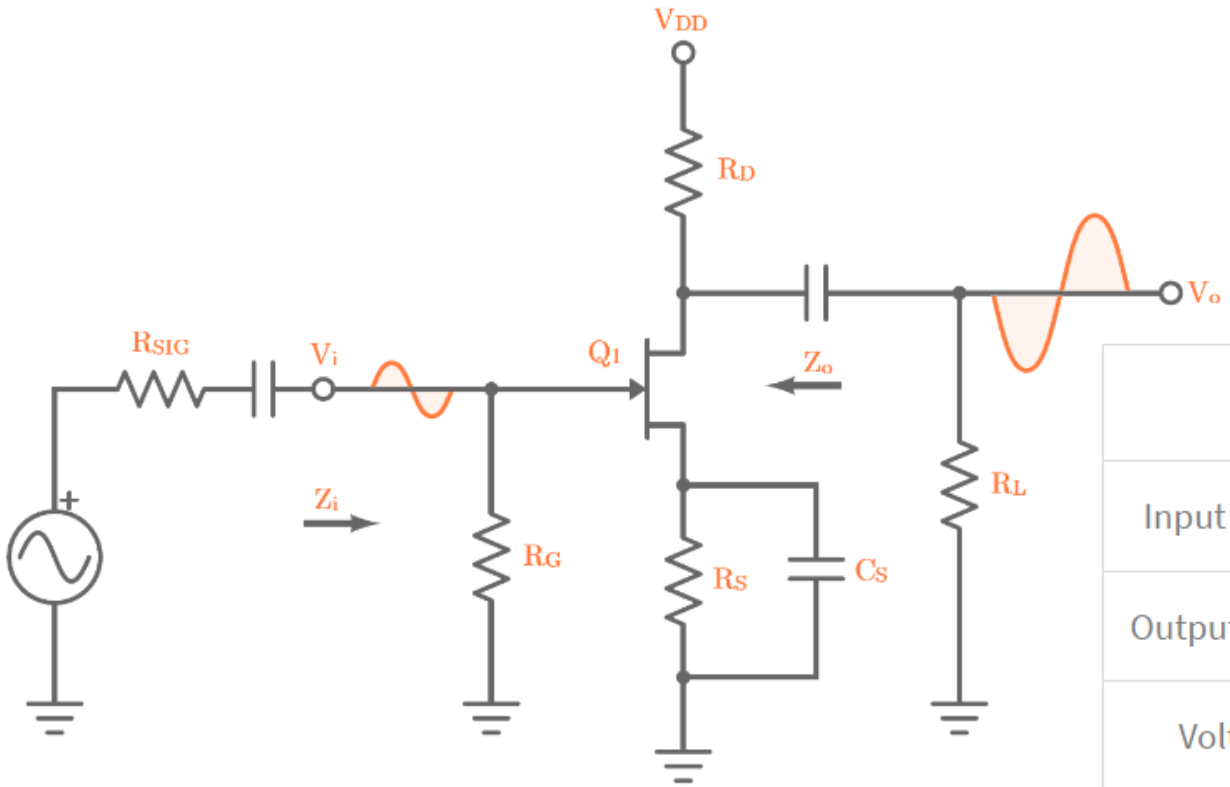
Input Impedance	$Z_i = R_1 \parallel R_2$	
Output Impedance	$Z_o = R_D \parallel r_d$	$Z_o \cong R_D \quad (r_d \geq 10R_D)$
Voltage Gain	$A_v = -g_m (r_d \parallel R_D)$	$A_v \cong -g_m R_D \quad (r_d \geq 10R_D)$

FET or D-MOSFET Common-Gate Configuration (No-Load)



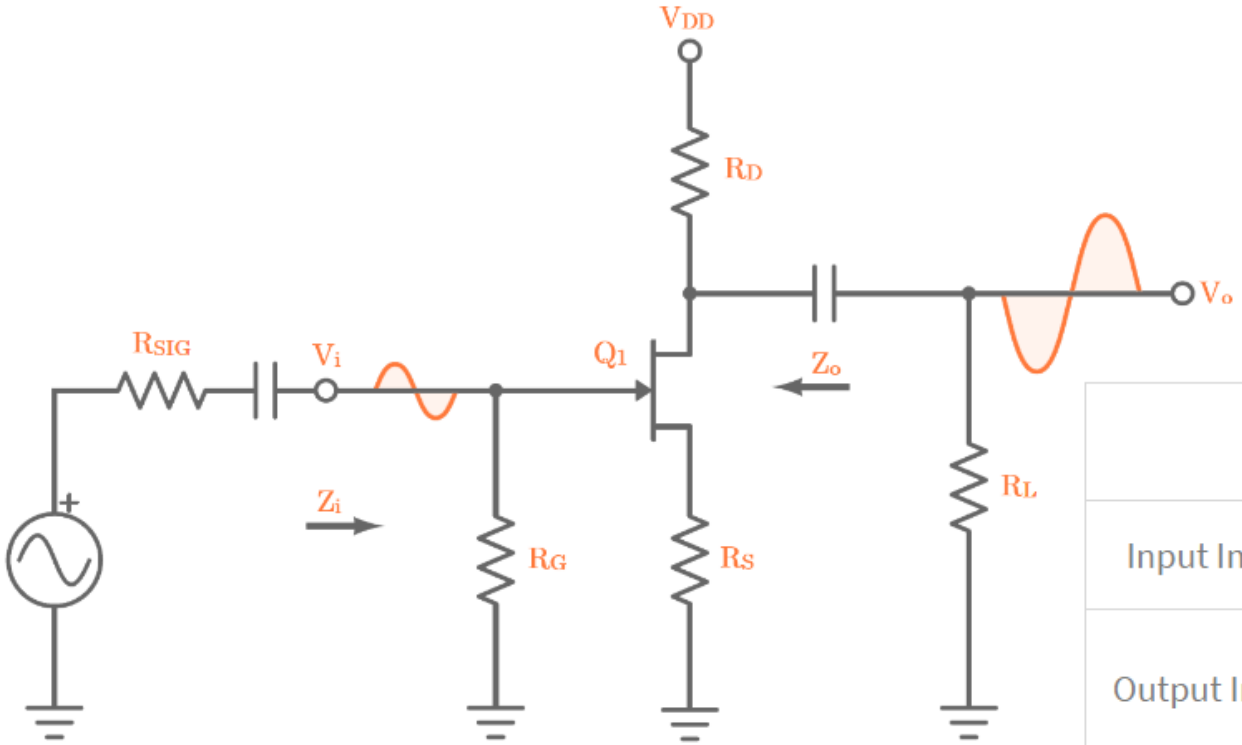
Input Impedance	$\mathrm{Z}_i = \mathrm{R_S} \parallel \left[\frac{\mathrm{r}_d + \mathrm{R_D}}{1 + g_m \mathrm{r}_d}\right]$	$\mathrm{Z}_i \cong \mathrm{R_S} \parallel \frac{1}{g_m} \quad (\mathrm{r}_d \geq 10\mathrm{R_D})$
Output Impedance	$\mathrm{Z}_o = \mathrm{R_D} \parallel \mathrm{r}_d$	$\mathrm{Z}_o \cong \mathrm{R_D} \quad (\mathrm{r}_d \geq 10\mathrm{R_D})$
Voltage Gain	$\mathrm{A}_v = \frac{g_m \mathrm{R_D} + \frac{\mathrm{R_D}}{\mathrm{r}_d}}{1 + \frac{\mathrm{R_D}}{\mathrm{r}_d}}$	$\mathrm{A}_v \cong g_m \mathrm{R_D} \quad (\mathrm{r}_d \geq 10\mathrm{R_D})$

JFET Self-Bias Configuration Bypassed RS (with R_SIG and R_L)



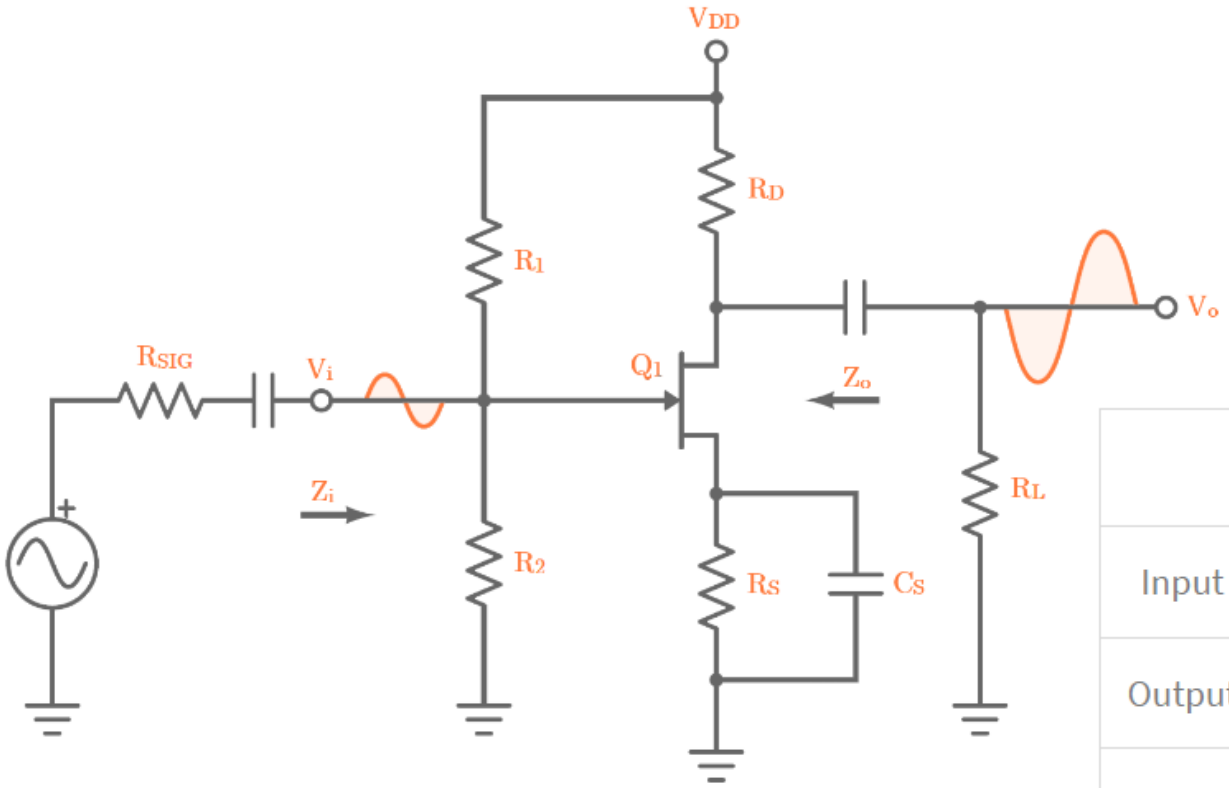
	Without r_d	With r_d
Input Impedance	$Z_i = R_G$	$Z_i = R_G$
Output Impedance	$Z_o = R_D$	$Z_o = R_D \parallel r_d$
Voltage Gain	$A_{v_L} = -g_m (R_D \parallel R_L)$	$A_{v_L} = -g_m (R_D \parallel R_L \parallel r_d)$

JFET Self-Bias Configuration Unbypassed R_S (with R_SIG and R_L)



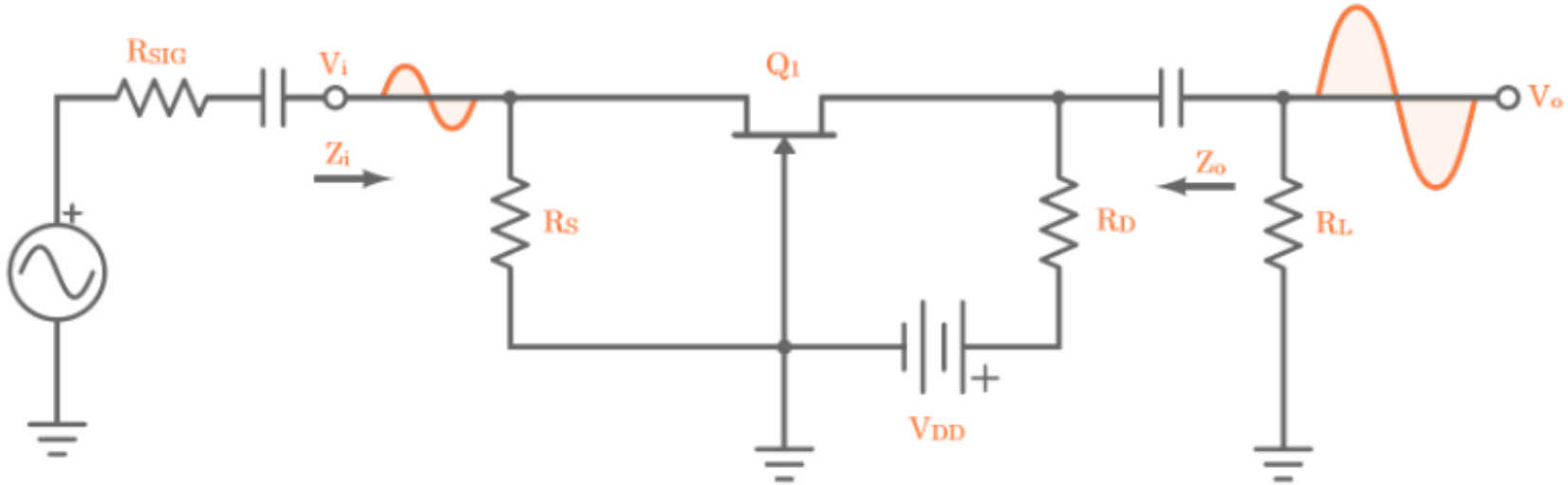
	Without r_d	With r_d
Input Impedance	$\mathrm{Z}_i = \mathrm{R_G}$	$\mathrm{Z}_i = \mathrm{R_G}$
Output Impedance	$\mathrm{Z}_o = \dfrac{\mathrm{R_D}}{1 + g_m \mathrm{R_S}}$	$\mathrm{Z}_o \cong \dfrac{\mathrm{R_D}}{1 + g_m \mathrm{R_S}}$
Voltage Gain	$\mathrm{A}_{v_\mathrm{L}} = -\dfrac{g_m \left(\mathrm{R_D} \parallel \mathrm{R_L}\right)}{1 + g_m \mathrm{R_S}}$	$\mathrm{A}_{v_\mathrm{L}} = -\dfrac{g_m \left(\mathrm{R_D} \parallel \mathrm{R_L}\right)}{1 + g_m \mathrm{R_S} + \frac{\mathrm{R_D} + \mathrm{R_S}}{r_d}}$

JFET Voltage-Divider Bias Configuration (with R_SIG and R_L)



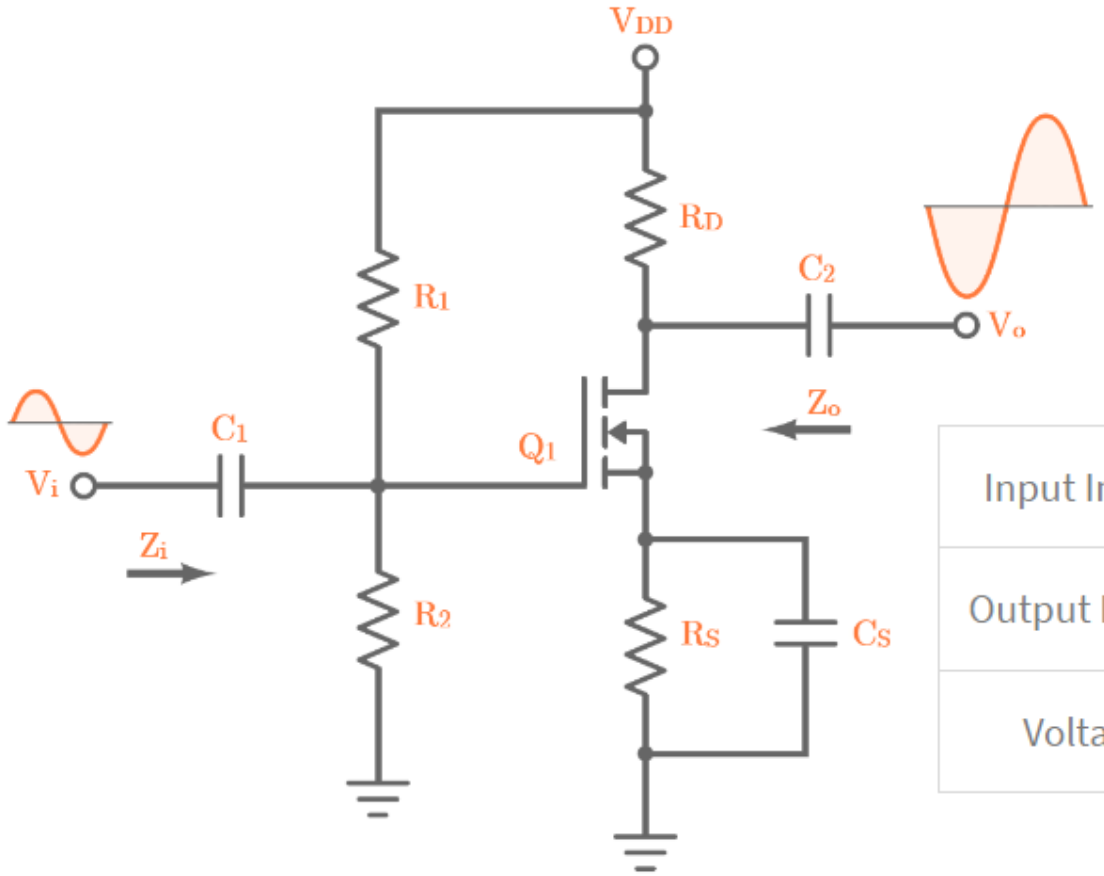
	Without r_d	With r_d
Input Impedance	$Z_i = R_1 \parallel R_2$	$Z_i = R_1 \parallel R_2$
Output Impedance	$Z_o = R_D$	$Z_o = R_D \parallel r_d$
Voltage Gain	$A_{v_L} = -g_m (R_D \parallel R_L)$	$A_{v_L} = -g_m (R_D \parallel R_L \parallel r_d)$

JFET AC Analysis: Common-Gate Configuration (with R_SIG and R_L)



	Without r_d	With r_d
Input Impedance	$Z_i = \frac{R_S}{1 + g_m R_S}$	$Z_i = \frac{R_S}{1 + \frac{g_m r_d R_S}{r_d + (R_D \parallel R_L)}}$
Output Impedance	$Z_o = R_D$	$Z_o = R_D \parallel r_d$
Voltage Gain	$A_{v_L} = g_m (R_D \parallel R_L)$	$A_{v_L} \cong g_m (R_D \parallel R_L)$

E-MOSFET Voltage-Divider Bias Configuration (No load)



Input Impedance	$\mathrm{Z}_i = \mathrm{R}_1 \parallel \mathrm{R}_2$	
Output Impedance	$\mathrm{Z}_o = \mathrm{R}_\mathrm{D} \parallel \mathrm{r}_d$	$\mathrm{Z}_o \cong \mathrm{R}_\mathrm{D} \quad (\mathrm{r}_d \geq 10\mathrm{R}_\mathrm{D})$
Voltage Gain	$\mathrm{A}_v = -g_m \left(\mathrm{r}_d \parallel \mathrm{R}_\mathrm{D}\right)$	$\mathrm{A}_v \cong -g_m \mathrm{R}_\mathrm{D} \quad (\mathrm{r}_d \geq 10\mathrm{R}_\mathrm{D})$

Thanks for listening ☺

YALÇIN İŞLER

Assoc. Prof.