BME208 Logic Design and Circuits

Yalcin Isler, Ph.D.

About

- 6 ECTS course
 - 3 hours theory
 - 1 hour laboratory
- Attendance
 - Compulsory
- Wednesday
 - 09:20 12:30

Grading

- If laboratory_grade <= 70
 - FAIL with unattendance
- ELSE
 - SUCCESS depends on
 - 40% midterm
 - 60% final (or resit)

Contact information

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- Office hours
 - Wednesday: 12.45 13.30

Selected answers to some stupid questions

• YES,

- whatever you see in lectures before the mid-term exam are included in the mid-term exam.
- whatever you see in lectures before the excuse exam are included in the excuse exam and this exam may be harder than or similar to the mid-term exam.
- all contents are included in the final exam.
- all contents are also included in the resit exam and this exam may be harder than or similar to the final exam.
- NO,
 - I will NOT give 1 point extra to you. You will take which grade you deserve.

Thanks

Yalcin ISLER, Ph.D.